# Processor Architecture From Dataflow To Superscalar And Beyond

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Processor Architecture From Dataflow To
Also consider the dataflow within the video processor and to off-chip storage. Finally, make sure that your architecture can achieve the required real-time performance for a worst-case bitstream with ...

Processor Architecture for High Performance Video Decode
One of the features of DSP Builder is the ability package these dataflow systems into co-processing ... When the FPGA co-processor was added to the system architecture, the total TI clock cycles ...

Developing and Integrating FPGA Co-processors with the TiC6X Family of DSP Processors
Melco Audio has announced a new high-capacity digital music library. The N100-H50 benefits from a 150 per cent capacity increase over the standard 2TB N100-H20, which stays in the brand ' s range, to ...

Melco adds N100-H50 5TB Digital Music Library
A better way to design the architecture ... CPU utilization to be less than 0.743 in order to ensure that our tasks can be scheduled. (Keep in mind that RMS comes with a lot of assumptions but it ' s a ...

Developing an RTOS Application Software Architecture
Leading semiconductor test equipment supplier Advantest Corporation (TSE: 6857) is pilot testing a next-generation solution ...

Advantest Developing Innovative Methodologies for High-Speed Scan and Software-Based Functional Testing
novel non-von-Neumann processor architectures and their programming methods where algorithms are mapped onto data-flow

circuits. Conduct research regarding processors, computing systems, programing ...

Seeking a Research Scientist or Postdoctoral Researcher (R-CCS2105)
Melco Audio has significantly upgraded its highly acclaimed entry-level N100-H20 digital music library, creating a new high-capacity HDD variant, the N100-H50, which more than doubles the original ...

Melco announces the new N100-H50, its best ever entry-level digital library with 150 % more music capacity
NVidia's new Kepler architecture targets embedded applications ... be handled efficiently by the GPUs. Likewise, data flow takes longer with CPU/GPU interaction because of synchronization issues.

GPU Architecture Improves Embedded Application Support
As with data flow, the 'C67x relies on external ... innovate effective methods of achieving inter-processor communications. Spectrum's FastTrack architecture is an example of this, using a ...

Factors To Consider When Choosing The Right DSP For The Job
NVIDIA ' s GPUs dominate AI chips. But a raft of startups say new architecture is needed for the fast-evolving AI field ...

NVIDIA and the battle for the future of AI chips
TOPS, 3-TOPS per Watt Hailo-8 NPU on two fanless edge computers running Linux: the Coffee Lake and PCIe equipped LEC-2290 and the compact, Apollo Lake based LEC-7242.

Hailo-8 NPU ships on Linux-powered Lanner edge systems
the data flow and total system throughput are improved to enhance the performance of the workload. The NVIDIA ® Tesla ® V100 accelerator is built for HPC and deep learning, and is based on NVIDIA ' s new ...

Achieving Maximum Compute Throughput: PCIe vs. SXM2
You can handle even the most complex scenarios of async data flow using the nested observables and the various flattening strategies provided by RxJS. One of the most challenging aspects of ...

Deep Dive into Reactive Programming with RxJS
On the hardware front, artificial intelligence is locked into its own personal Game of Thrones, with different houses all vying for supremacy and to create the chip architecture that ... numerical ...

The Battle of AI Processors Begins in 2018

Instead of just one monolithic chip developed at a single process node, many of the most advanced architectures incorporate multiple ... design their own hardware to optimize their particular data ...

The Increasingly Uneven Race To 3nm/2nm

AI has been a hot topic recently, especially this week. With all the efforts coming out, there is a growing need for better hardware, collaborating, and easing deployment. Just this week alone, AI has ...

Supporting the AI Boom: Facing the Challenges of Hardware and Deployment

Ball Aerospace provided the event-driven architecture for dealing with the ... and not having to haul in a bunch of processors, and not having to haul in a bunch of storage, and having that ...

Microsoft and Ball Aerospace enlist the cloud to speed up Space Force ' s data flow

Arteris IP functional safety manager Stefano Lorenzini recently presented " Automotive Systems-on-Chip (SoCs) with AI/ML and Functional Safety " at the Linley Processor Conference ... deal with the ...

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