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It was both non-trivial and used the board's features nicely. But it has the message hard coded into the Verilog which means you need to rebuild the FPGA every time you want to change it.

Download File PDF Verilog Nonblocking Ignments With Delays Myths Mysteries How To Add UART To Your FPGA Projects

Some of the guidelines which designer needs to follow to make the design synthesizable are:

- Infer registers
- Avoid combinational feedback loops
- Specify complete sensitivity list to avoid ...

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Enforcing Design Rules to Develop
Reusable IP

At this level, the channels are blocking
and nonblocking I/O. No cycle-
accurate and pin-accurate ... This kind
of simulation may be timed with delay

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Annotations and may use the
simulation environment ...

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